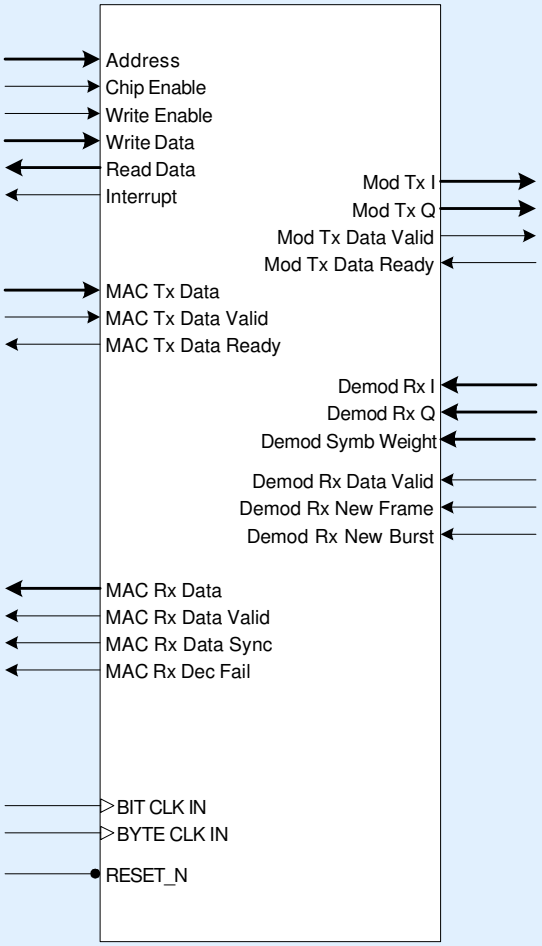
802.16 Channel Codec

CMS0005

- Fully compliant with the 802.16a WirelessMAN-OFDM-Phy Layer Specification.
  - QAM Mapping and Demapping
  - Interleaving/De-interleaving
  - Convolutional Encoder/Viterbi Decoder
  - Reed-Solomon Encoder/Decoder
  - Randomiser/De-randomiser
- Simple MAC management of burst profile changes within the upstream and downstream channels.
- Advanced Error Control capability using Symbol Weight inputs.



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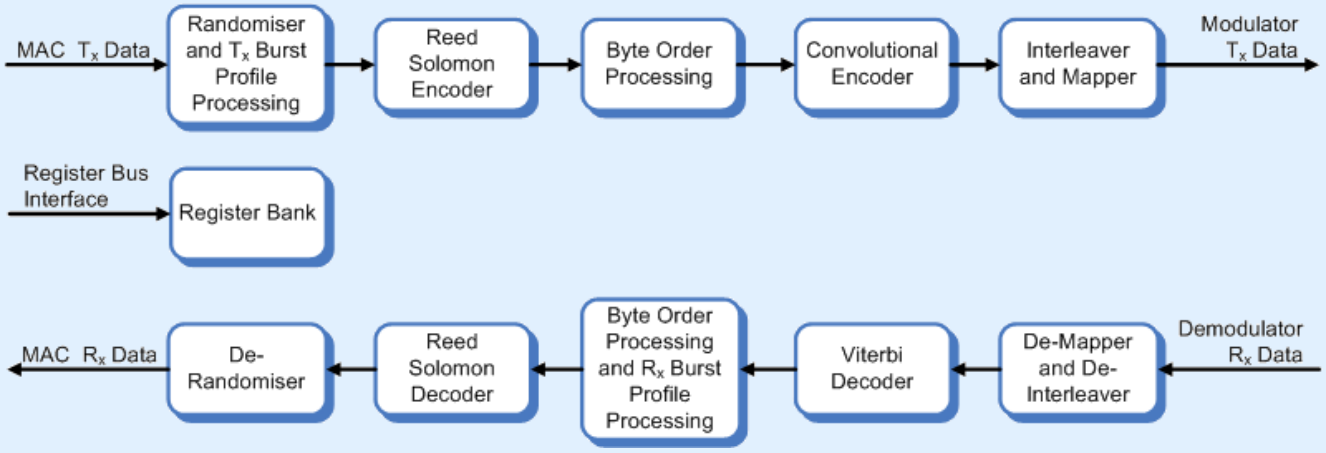
Block Diagram



Detailed Description

The Commsonic CMS0005 802.16 Channel Codec provides all of the functionality necessary to implement the back end data processing in an 802.16a WirelessMAN-OFDM Phy Layer device. Its design has been carefully constructed to provide excellent FPGA performance without compromising the ASIC implementation in terms of area or speed.

A description of the processing steps follows:

Randomiser. This block implements the 802.16 randomisation function $1+x^{14}+x^{15}$. In addition it controls the burst profiling of the transmitter and zero-tail byte insertion specified by 802.16a. The burst profile can be any of the QAM orders and coding rates that are specified by 802.16a. The burst profile control requires the MAC software to write the specifications of the bursts into a FIFO within the register bank. Once the randomiser has the burst profile it will request data from the MAC at a rate determined by the front end of the modulator.

Reed-Solomon Encoder. This block will generate Reed Solomon packets based on the burst profile supplied by the randomiser.

Transmit Byte Order Processing. 802.16a specifies that the Reed-Solomon parity bytes be transmitted before the payload in order that the zero tail-byte inserted by the scrambler is kept at the end of the packet. This block handles this reversal in addition to converting the byte stream to the bit stream required by the Convolutional Encoder.

Convolutional Encoder. This block performs the zero-terminating convolutional encoding as specified by 802.16a.

Interleaver, Mapper. 802.16a specifies a block interleaver in a two-step permutation. These blocks perform that interleaving in addition to the QAM constellation mapping. It outputs I/Q QAM symbols to the modulator.

Demapper, De-interleaver. These blocks perform the soft decision demapping of the I/Q samples from the demodulator. In addition, they perform the de-puncturing function required by the Viterbi Decoder.

Viterbi Decoder. This block performs the Viterbi Decoding function with zero-flush as specified by 802.16a. For further details on this block see the separate data sheet for CMS0002, the Commsonic Viterbi Decoder.

Receive Byte Order Processing & Burst Profile Processing. This block takes the bit-stream input from the Viterbi decoder and converts it to a byte stream before reversing the parity/payload order in order that the data is formatted correctly for receipt by the Reed-Solomon decoder. In addition, it manages the burst profiles used by the receiver. This includes extraction of the Frame Control Header (FCH) from the first OFDM symbol of a downstream frame and setting the parameters for the remainder of the receive chain to match the required QAM order and code rate. Settings for the burst following the FCH symbol are managed automatically; all other burst profile settings are programmed by software.

Detailed Description (Cont'd)

Reed-Solomon Decoder. This block will perform Reed-Solomon decoding and error correction of the received packets. For full details of this block see the Commsonic data sheet for the CMS0003, the Commsonic Reed Solomon Decoder.

De-Randomiser. This block applies the same randomising polynomial as the randomiser in order to recover the received data. In addition, it removes the zero tail-byte that was applied for the convolutional encoding/decoding. It outputs the received data stream delineated using the sync pulse.

Register Bank. The register bank provides a simple 32-bit interface for reading and writing registers within the FEC block. Full details of the registers within the FEC core are contained within the full data sheet.

Principle I/O Description

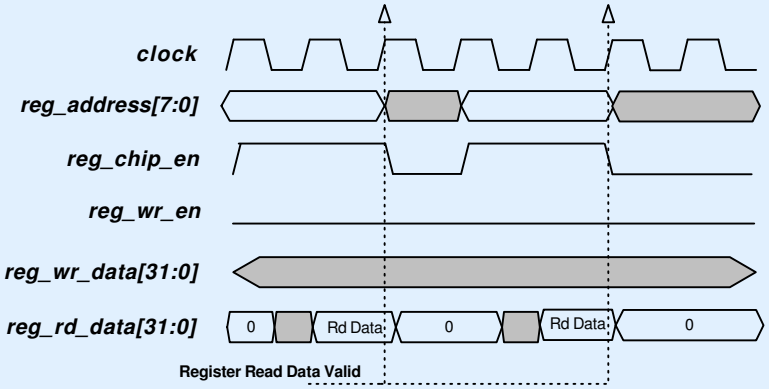
Register Bus Interface	
reg_address	Register address select input.
reg_chip_en	Block select input for the CMS0005 register bank.
reg-wr_en	Write Enable Input for block registers.
reg_wr_data	32-bit Write data input.
reg_rd_data	32-bit Read data output.
reg_irq	Core Interrupt.
MAC Interface	
MAC Tx Data	8-bit Transmit data input from MAC
MAC Tx Data Valid	Transmit data valid input
MAC Tx Data Ready	FEC Transmit path is ready for new byte. Data transferred when Ready and Valid are asserted together.
MAC Rx Data	8-bit MAC Receive demodulated and decoded data output.
MAC Rx Data Valid	Valid strobe for receive data.
MAC Rx Data Sync	Sync pulse for identifying receive data packet boundaries.
MAC Rx Decode Fail	Flag indicating that this packet failed RS Decode and should be discarded.
Demodulator/Modulator Interface	
Mod Tx I	4-bit Transmit I complex output
Mod Tx Q	4-bit Transmit Q complex output
Mod Tx Data Valid	Transmit data valid output strobe
Mod Tx Data Ready	Modulator is ready for new data sample. Data transferred on simultaneous assertion of Ready and Valid.
Demod Rx I	Complex I input from demodulator. Number of bits can be set with a generic.
Demod Rx Q	Complex Q input from demodulator. Number of bits can be set with a generic.
Demod Symbol Weight	This input allows advanced error control based on estimated carrier reliability. Number of bits can be set with a generic.
Demod Rx Data Valid	Valid Strobe for receive data.
Demod Rx New Frame	Marks a symbol as being the first (non-preamble) in a new downstream frame.
Demod Rx New Burst	Marks a received symbols as being the first (non-preamble) in a new burst.
Others	
Bit Clock	Clock input for bit-processing functions, frequency at twice the sample rate.
Byte Clock	Clock input for byte-processing functions. Should be exactly half the frequency and in phase with the bit clock.
Reset_N	Asynchronous reset input

Register Interface

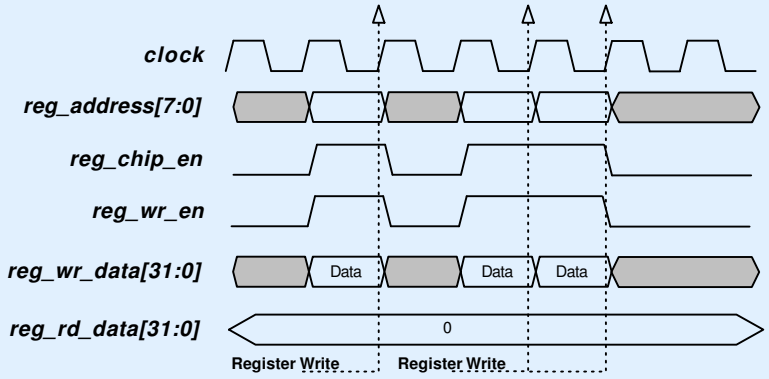
A simple 32-bit register-programming interface is provided. The register core is intended to be interfaced to whatever host interface is appropriate for the application (e.g. I^2C, 8-bit, big-endian, little-endian, etc). The register-core can be interface directly with the Altera SOPC builder via the Avalon bus using a zero wait-state configuration.

An active-high interrupt line is also available.

Register read access:

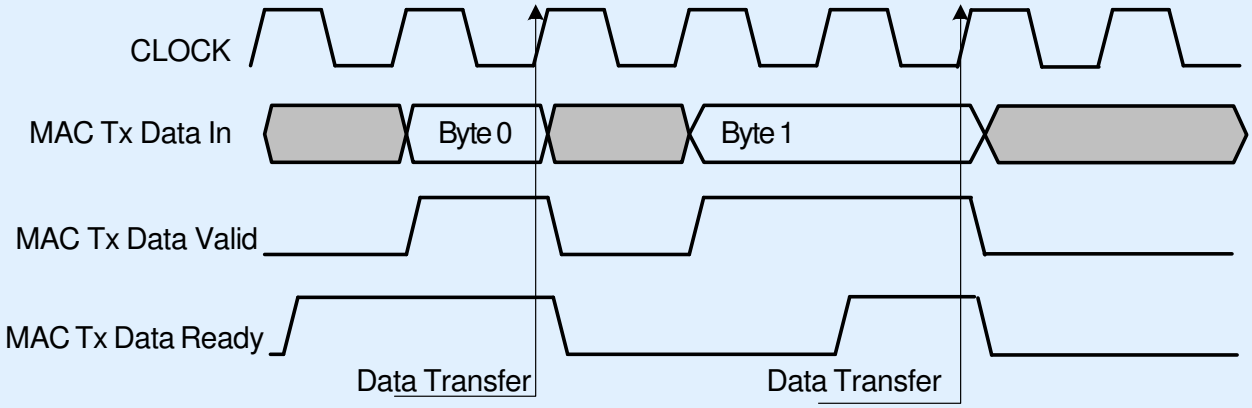


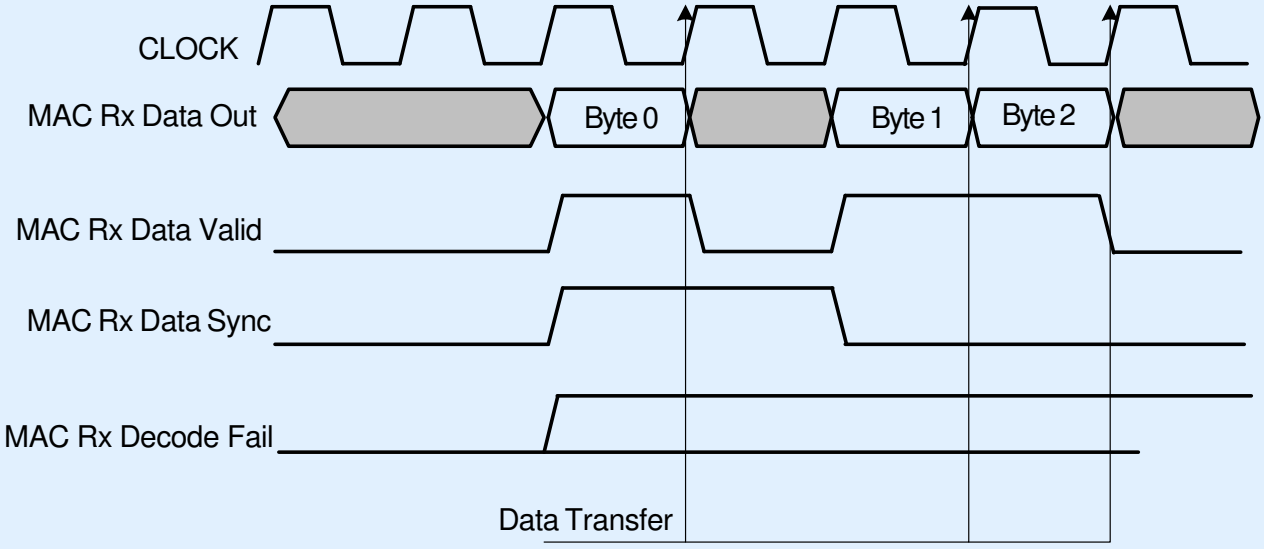
Register write access:



Timing Diagrams

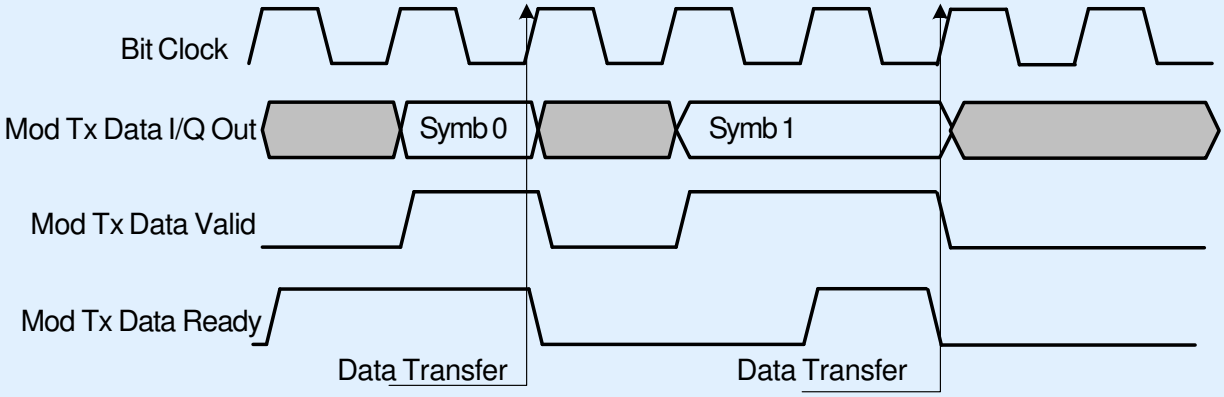
MAC Data Interface:

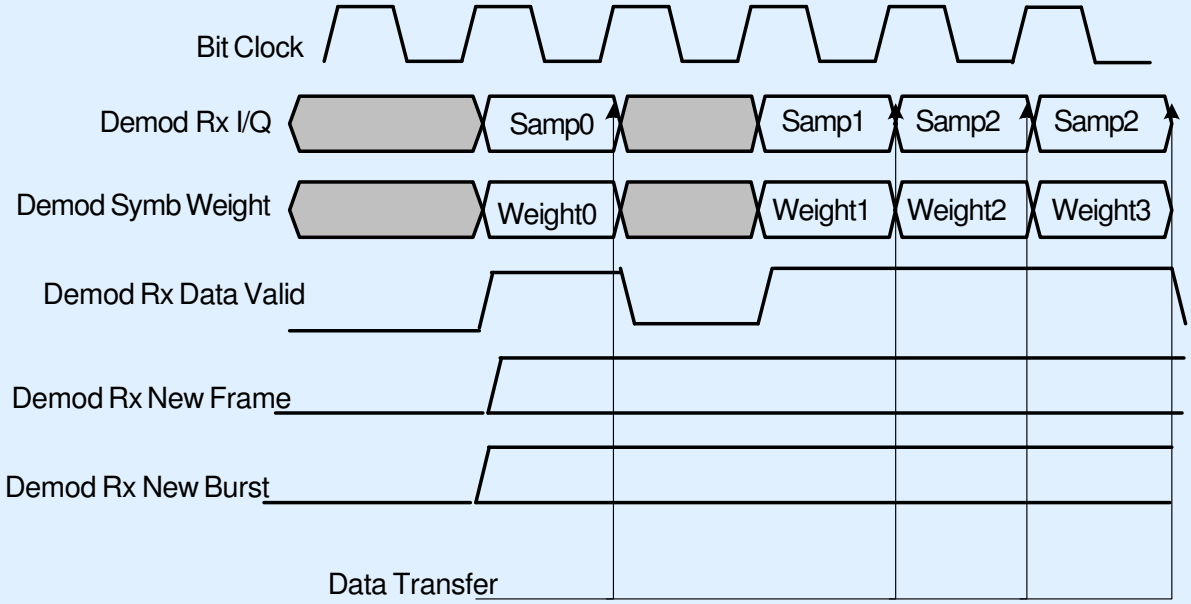




Timing Diagrams (Cont'd)

Modulator/Demodulator Data Interface:





About Commsonic:

Commsonic is an IP and design services company that specialises in the development of ASIC, FPGA, DSP and board-level sub-systems for applications in wireless and wireline communications.

Our expertise is primarily in the gate- and power-efficient implementation of physical-layer (PHY) functions such as modulation, demodulation and channel coding, but we have extensive experience with all of the major elements of a modern baseband 'core' including medium access control (MAC), voiceband DSP, mixed-signal interfaces and embedded CPU and software.

Our services are available on a turn-key basis but they are usually provided as part of a support package attached to members of our expanding family of licensable IP cores.

Commsonic's IP spans the major Standards for cable, satellite and terrestrial digital TV transmission and includes high-performance, adaptable, single-carrier (QAM) and multi-carrier (COFDM) modulator and demodulator solutions for DVB-S2, DVB-C/J.83/A/B/C and DVB-T/H.

Commsonic's customers are typically semiconductor vendors and manufacturers of broadband transceiver equipment that demand leading-edge Standards-based or proprietary PHY solutions but don't have the internal resources necessary to get their products to market soon enough.

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